AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Canceled)

2. (Currently Amended) The apparatus of claim [[1]] 33, wherein the voltage generating circuit comprises:

a capacitor; and wherein

the switching structure is configured to selectively store charges corresponding to the input voltage in the capacitor, and to selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

3. (Original) The apparatus of claim 2, wherein the control circuit is configured to generate the control current based on a difference between the boosted voltage and a desired boosted voltage.

4. (Currently Amended) The apparatus of claim [[1]] 33, wherein ~~the switching structure includes first, second, third and fourth switches; and~~ the voltage generating circuit further comprises:

a capacitor configured to store charges corresponding to the input voltage while the second and third switches are turned on, and outputting the boosted voltage while the first and fourth switches are turned on.

5. (Canceled).

6. (Currently Amended) The apparatus of claim [[5]] 33, wherein

the third clock signal has an inverted phase with respect to the first clock signal;

a front edge of the second clock signal is delayed by a fixed time with respect to a front edge of the first clock signal; and

an active period of the second clock signal is narrower than that of the first clock signal.

7. (Currently Amended) The apparatus of claim [[5]] 33, wherein the level shifter includes a metal-oxide silicon (MOS) capacitor.

8. (Currently Amended) The apparatus of claim [[5]] 33, wherein the switch control signal swings between the level of the input voltage and substantially double the level of the input voltage.

9. (Original) The apparatus of claim 8, wherein the fourth switch is turned on during a non-active status of the switching control signal, and the

third switch is turned on during an active status of the switching control signal.

10. (Currently Amended) The apparatus of claim [[1]] 33, wherein the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage.

11. (Currently Amended) The apparatus of claim [[1]] 33, wherein the control circuit is configured to generate the control current based on a difference between the boosted voltage and the desired boosted voltage.

12. (Currently Amended) The apparatus of claim [[1]] 33, wherein the control circuit comprises:

a voltage divider configured to generate a divided voltage from the boosted voltage;

a comparator configured to compare the divided voltage with a reference voltage; and

a current generator configured to generate the control current based on output from the comparator.

13. (Original) The apparatus of claim 12, wherein the reference voltage represents a desired boosted voltage.

14. (Currently Amended) The apparatus of claim [[1]] 33, wherein the control circuit comprises:

a voltage divider configured to divide the boosted voltage to generate a divided voltage;

an amplifier configured to amplify a difference voltage between a reference voltage and the divided voltage; and

a voltage controlled current source configured to generate the control current based on the amplified difference voltage.

15. (Original) The apparatus of claim 14, wherein the reference voltage represents a desired boosted voltage.

16. (Original) The apparatus of claim 14, wherein voltage controlled current source decreases the control current when the divided voltage is higher than the reference voltage, and increases the control current when the divided voltage is lower than the reference voltage.

17. (Currently Amended) A method for controlling a boosted voltage, comprising:

generating a boosted voltage from an input voltage based on a control current and charges stored in a charge storing element, the generating of a boosted voltage including,

generating first, second and third clock signals, ~~output from a clock signal generator;~~

selectively changing a level of the input voltage based on the third clock signal~~output~~ from the clock signal generator,

~~selectively~~ storing [[the]] charges corresponding to the input voltage in the charge storing element when a second and third switch are turned on and ~~selectively~~ outputting the stored charges in conjunction with charges corresponding to a control current as the boosted voltage ~~based on output from the clock signal generator and the selectively changed level of the input voltage~~ when first and fourth switches are turned on, the first and second switches being turned on in response to the first and second clock signal, and the third and fourth switches being turned on in response to a switching control signal, the switching control signal being generated based on the third clock signal;

generating the control current based on the boosted voltage; and

supplying the control current for generating the boosted voltage while the charges stored in the charge storing element are used to generate the boosted voltage.

18. (Canceled)

19. (Previously Presented) The method of claim 17, wherein the generating the control current step generates the control current based on a difference between the boosted voltage and a desired boosted voltage.

20. (Original) The method of claim 17, wherein the generating the control current step generates the control current based on the boosted voltage and a desired boosted voltage.

21. (Original) The method of claim 20, wherein the generating the control current step generates the control current based on a difference between the boosted voltage and the desired boosted voltage.

22. (Original) The method of claim 17, wherein the generating the control current step comprises:

generating a divided voltage from the boosted voltage by dividing the boosted voltage;

a comparing the divided voltage with a reference voltage; and

generating the control current based on output from the comparing step.

23. (Original) The method of claim 22, wherein the reference voltage represents a desired boosted voltage.

24. (Original) The method of claim 17, wherein the generating the control current step comprises:

dividing the boosted voltage to generate a divided voltage;

amplifying a difference voltage between a reference voltage and the divided voltage; and

generating the control current based on the amplified difference voltage.

25. (Original) The method of claim 24, wherein the reference voltage represents a desired boosted voltage.

26. (Previously Presented) The apparatus of claim 2, wherein the switching structure is configured to selectively receive the control current while configured to selectively output the stored charges.

27. (Previously Presented) The apparatus of claim 26, wherein the switching structure includes a switch configured to selectively connect a portion of the control circuit generating the control current with the capacitor.

28. (Previously Presented) The apparatus of claim 2, wherein the voltage generating circuit is configured to not receive the control current when charges are stored in the capacitor.

29. (Previously Presented) The apparatus of claim 4, wherein the first switch is configured to connect a portion of the control circuit generating the control current with the capacitor when turned on.

30. (Currently Amended) The apparatus of claim [[5]] 33, wherein the first switch is configured to connect a portion of the control circuit generating the control current with the capacitor when turned on.

31. (Previously Presented) The apparatus of claim 30, wherein

the third clock signal has an inverted phase with respect to the first clock signal;

a front edge of the second clock signal is delayed by a fixed time with respect to a front edge of the first clock signal; and

an active period of the second clock signal ends before that of the first clock signal.

32. (Canceled)

33. (Currently Amended) An apparatus for controlling a boosted voltage, comprising:

a voltage generating circuit configured to generate a boosted voltage from an input voltage based on a control current and charges stored in a charge storing element, and configured to receive the control current while the charges

stored in the charge storing element are used to generate the boosted voltage; and

a control circuit configured to generate the control current based on the boosted voltage; wherein

the voltage generating circuit further includes,

a clock signal generator configured to generate first, second and third clock signals,

a level shifter circuit configured to selectively change a level of the input voltage in response to the third clock signal to output a switching control signal, and wherein

first and second switches [[are]] switched in response to the first and second clock signals, and

third and fourth switches [[are]] switched in response to [[a]] the ~~switch~~ switching control signal.